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Application Number	09/915,188
Filing Date	July 25, 2001
First Named Inventor	John C. Dute' et al.
Art Unit	2154
Examiner Name	Jungwon Chang
Attorney Docket Number	1-16437

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
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AMENDED APPEAL BREIF

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MARSHALL & MARSHALL LLC.		
Signature	Stephen G. Kimmet		
Printed name	Stephen G. Kimmet		
Date	January 12, 2007	Reg. No.	52,488

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: John C. Dute' et al.	)	Group Art Unit: 2154
Serial No.: 09/915,188	)	Examiner: Jungwon Chang
Filing Date: July 25, 2001	)	Attorney Docket: 1-16437
For: System, Device and Method for Comprehensive Input/Output Interface Between Process or Machine Transducers and Controlling Device or System	)	

January 12, 2007

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
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AMENDED BRIEF ON APPEAL

Honorable Sir:

This amended brief is being filed in response to the Notice of Non-Compliant Appeal Brief of December 14, 2006. This amended brief will replace all previous briefs and amended briefs. The first paragraph of the Summary (page 4), the Evidence Appendix, and the Related Proceedings Appendix have been amended. It is appellants' understanding that no fee(s) is required.

1. Real Party in Interest

The real party in interest is Electronic Solutions, Inc. The assignment to Electronic Solutions, Inc., was recorded on November 10, 2003, at reel 014677, frame 0935.

2. Related Appeals and Interferences

There is no known related appeal or interference that will directly affect or be directly affected by, or have a bearing on, the Board's decision in this Appeal.

3. Status of Claims

The status of each of the claims is as follows:

1) Claims canceled: 1-85

2) Claims withdrawn from consideration but not canceled: None

3) Claims pending: 86-90

4) Claims allowed: None

5) Claim objected to: 86

6) Claims rejected: 86-90

The claims on appeal are 86-90.

A copy of the claims on file is submitted in the attached Claims Appendix.

4. Status of Amendments

No amendment was filed subsequent to the final rejection of the application by the Office Action of August 8, 2005.

5. Summary of Claimed Subject Matter

The present invention, as defined in independent claim 86, defines a comprehensive interface circuit (see, for example, Fig. 1) for simultaneously (see, for example, page 3, lines 14-15) sensing input devices (70) and output devices (72) that comprises a first physical circuit package (15) (see, for example, page 4, lines 21-22) having a first electrical terminal (101-T_1), a second electrical terminal (102-T_2), and a plurality of mode circuits (16) (see, for example, page 4, lines 4-12) disposed thereon.

The plurality of mode circuits (16) can accomplish digital input, digital output, analog input, and analog output (see, for example, page 3, lines 27-30). The first physical circuit package (15) is electrically connected (74,75 exclusive-or 76,77) directly, exclusively, and physically to a single sensor (70) or a single actuator (72), but not both (74,75 or 76,77) simultaneously (see, for example, page 4, lines 4-6), via only (see, for example, page 4, lines 16-17) the first electrical terminal (101-T_1) and the second electrical terminal (102-T_2) of the first physical circuit package (15). The first electrical terminal (101-T_1) and the second electrical terminal (102-T_2) are capable of electrical communication with each of the plurality of mode circuits (16).

The present invention further comprises a second physical circuit package (15) (see, for example, page 2, lines 4-6 – thus, each package (15) having the same reference item numbers) having a first electrical terminal (101-T_1), a second electrical terminal (102-T_2) and a plurality of mode circuits (16) disposed thereon. The second plurality of mode circuits (16) can accomplish digital input, digital output, analog input, and analog output. The second physical circuit package (15) is electrically connected directly, exclusively, and physically to another single sensor (70) or another single actuator (72), but not both simultaneously, via only the first electrical terminal (101-T_1) and the second electrical terminal (102-T_2) of the second physical circuit package (15), and the first electrical terminal (101-T_1) and the second electrical terminal (102-T_2) are capable of electrical communication with each of the plurality of mode circuits (16).

The present invention still further comprises a controller (14) that is external (see, for example, page 6, lines 13-16 and Fig. 1) to the first physical circuit package (15) and the second physical circuit package. The controller (14) is capable of simultaneously (see, for example, page 2, lines 4-6, page 2, lines 10-12, page 3, lines 14-15, and Fig. 1) receiving a condition from each sensor (70) and is capable of simultaneously (see, for example, page 2, lines 4-6, page 2, lines 10-12, page 3, lines 14-15, and Fig. 1) sending commands to each actuator (72).

6. Grounds of Rejection/Objection to be Reviewed on Appeal

The issues for appeal are:

a) The drawings are objected to under 37 CFR 1.83(a), as the drawings must show every feature of the invention specified in the embodiment of claim 86.

b) The specification is objected to under 37 CFR I.75(d)(1) and MPEP § 608.01(o), as it applies to the embodiment of claim 86.

c) Claims 86-90 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

d) Claims 86-90 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

e) Claims 86-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLeish (U.S. Patent No. 5,014,238, hereinafter McLeish) in view of Sitte (U.S. Patent No. 5,469,150, hereinafter Sitte).

7. Argument

a) In regard to the "Grounds of Rejection" section 6a, which is the objection to the drawings under 37 CFR 1.83(a), the Examiner asserts that the drawings must show two physical circuit packages and a single controller, which are claimed in claim 86.

Applicants assert that Fig. 1 shows how a physical circuit package 15 and a single controller 14 are connected together and that there is no reason to show how cumulative physical circuit packages 15 are connected to the same controller 14, since one skilled in the art recognizes how additional physical circuit packages are connected to the single controller 14. Applicants' position is founded in the fact that a programmable logic controller (PLC) has been utilized to interface multiple interface cards (e.g., two physical circuit packages 15), which have been individually and separately connected to a PLC (and for that matter a computer), since the 1969 development of the first PLC (see, for example, page 2, line 11).

A discovery, however, of the claimed invention is that each of the physical packages is electrically connected to an individual/separate sensor or to an individual/separate actuator via only the same two individual terminals 101-T_1 and 102-T_2.

For all of these reasons, applicants respectfully submit that the drawings do show the claimed invention and do meet all of the requirements of 37 C.F.R. 1.83(a).

b) In regard to the "Grounds of Rejection" section 6b, which is the objection to the specification under 37 CFR 1.75(d)(1) and MPEP § 608.01(o), the Examiner asserts that the specification fails to provide proper antecedent basis for the claimed subject matter, since it appears to the Examiner that the specification does not disclose the embodiment of claim 86, which has two physical circuit packages and a single controller.

Applicants traverse this objection by asserting that the disclosure of the present invention and common knowledge in the art, provide for every feature of the claimed invention.

In support of applicants' assertions, applicants find that at least Fig. 1 and the specification (see, for example, page 2, lines 4-6), disclose a physical circuit package 15 being electrically connected directly, exclusively, and physically to a single sensor 70 or a single actuator 72, but not both simultaneously. The physical circuit package 15 is also in electrical communication with an external controller 14. As so described, applicants note that this is a common wiring means in the art, as stated in detail in Argument section 7a.

However, a discovery of the claimed invention is that mode circuits 16 with point controller 12 are disposed within each physical circuit package 15 and that the electrical connectivity between a physical circuit package 15 and each sensor 70 or each actuator 72 is by way of only the same two individual terminals 101-T_1 and 102-T_2.

Below, applicants cite specific locations within the disclosure that support at least parts of the claimed invention of claim 86:

> "In one embodiment, the inventive interface and method includes and needs only two terminals for the connection of a sensor or actuator ..." (page 4, lines 16-17);

internally the physical circuit package 15 may "send or receive analog or digital voltage and/or current inputs... " (page 3, lines 27-30) by way of mode circuits 16;

"a ... controller with a sensor monitoring ... or an actuator acting ..." (page 4, lines 4-6);

"an individual electronic interface (15) between a controller (14) and each of the sensors and actuators of the process or machine being controlled" (page 2, lines 4-6);

the external controller may be a PLC (programmable logic controller) (see, for example, page 2, lines 10-12); and

the external controller may be a computer (see, for example, page 6 lines 13-16).

Thus, the claimed invention of claim 86 comprises individual physical circuit packages that need only two terminals to simultaneously connect each sensor monitoring or each actuator acting to an external controller.

Applicants postulate that if each sensor and each actuator always required a separate PLC or a separate computer, then the automated process or machine associated with those sensors and actuators would be applying a very ineffective use of computing resources.

For all of these reasons, applicants respectfully submit that the disclosure of the present invention does disclose the embodiment of claim 86, does provide antecedent basis for the claimed subject matter, and meets all of the requirements of 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

However, since this is the first time that these objections have been made in the present application, and if it were to please the Board to require drawing changes and/or specification changes, applicants would consider those drawing changes and/or specification changes.

c) In regard to the "Grounds of Rejection" section 6c where claims 86-90 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, the Examiner asserts that these claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the Examiner asserts that claim 86 recites two physical circuit packages in simultaneous communication with a single controller.

The Examiner asserts that no reference can be found to this embodiment in the disclosure as originally filed, which (as the Examiner asserts) applicants have cited as page 3, lines 4-12, in support of "simultaneously" receiving a condition from a sensor and sending commands to an actuator. However, the Examiner further asserts that this

passage refers to the sensing of inputs and outputs by a single physical circuit package of the invention and makes no reference to the controller.

Furthermore, the Examiner continues by asserting that the disclosure does not indicate that the controller itself receives conditions from the sensor and sends commands to the actuator, but rather, this function is disclosed as performed by the physical circuit package. The Examiner then goes on to assert that the controller is disclosed only as receiving status data from and sending command data to the physical circuit package (see pg. 6, lines 25-28). The Examiner continues by asserting that even if the point controller can be construed as performing these functions, the point controller is claimed as being part of the physical circuit package and not part of the recited "controller." The Examiner goes on to refer to claim 87 and concludes from this that, therefore, the disclosure also fails to provide proper support for a controller which is capable of receiving condition data from a sensor and sending commands to an actuator, irrespective of whether these sending/receiving functions are performed "simultaneously."

Moreover, the Examiner continues by asserting that the passage cited page 3, lines 4-12, of the specification is in direct contradiction to the limitation that each physical circuit package is "electrically connected directly, exclusively, and physically to a single sensor or a single actuator, but not both simultaneously." From this the Examiner asserts that the passage clearly implies that each physical circuit package is in fact capable of being connected to at least one sensor (input) and one actuator (output) simultaneously.

It is the Examiner's conclusion that Fig. 1 illustrates just such an embodiment and that the disclosure makes no mention of a circuit which is limited to exclusively being connected to only one of a sensor or an actuator. Therefore, the Examiner asserts that the disclosure also fails to provide proper support for this limitation of the claims.

Applicants, however, traverse these rejections by asserting that claims 86-90 do comply with the written description requirement and do contain subject matter which is described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Specifically, in regard to the Examiner's assertions that the specification does not disclose two physical circuit packages in simultaneous communication with a single controller, and that the Examiner cannot find any references to the embodiment of claim 86, applicants first refer the Board to applicants' responses in the above-stated Argument sections 7a and 7b, as those responses apply to these rejections under 35 USC 112, first paragraph.

Secondly, applicants refer the Board to applicants' Amendment dated May 6, 2005 where at page 5, line 18 applicants clearly cited page 3, lines 14-15, and also in said Amendment at page 6, lines 12-13 applicants clearly cited page 3, lines 14-15 and page 4, lines 4-12. However, in the Office Action of August 8, 2005, it appears to applicants

that the Examiner has incorrectly based these 35 U.S.C. 112 first paragraph rejections on the disclosure at page 3, lines 4-12 of the present application.

Applicants assert that the claimed invention of claim 86 is based upon the disclosure, at the time the application was filed, where it states "Thus, there is a need for a universal or comprehensive interface that ... permits simultaneous sensing inputs and outputs (page **3**, lines 10, 14, and 15)." Note that the conjunctive word "and" is taken to mean that the comprehensive interface circuit (see preamble of claim 86) indeed simultaneously senses inputs and outputs. In addition, this embodiment of the claimed invention of claim 86 is a predominant conventional configuration utilized with a PLC and a computer that applicants discussed above in Argument sections 7a and 7b.

The following are applicants' responses to subsequent speculations that the Examiner posed in the Office Action of August 8, 2005, which were based on the incorrect citation of page **3**, lines 4-12:

By way of the physical circuit package 15, which comprises the mode circuits 16, applicants assert that the controller 14 does receive conditions (i.e., monitoring) from the sensors and sends commands (i.e., actions) to the actuators (see, for example, page 4, lines 4-6). Also, as it is known by one skilled in the art, the status data received by the controller contains the conditions from the sensors and the sending command data from the controller contains the commands to the actuators.

Applicants assert that the external controller 14 is not to be construed as the point controller 12, the external controller is indeed external to the physical circuit package 15, and the point controller of claim 87 is indeed the point controller 12.

Applicants assert that the interface referred to at page 3, line 14 is the comprehensive interface circuit (see preamble of claim 86), which is capable of simultaneously sensing inputs and outputs of separate physical circuit packages.

In regard to the Examiner's speculations of "contradiction to the limitation" (which is based upon the improper citation of page 3, lines 4-12), applicants response to this assertion is that the applicants do recognize that the subject application does disclose other embodiments, but applicants reconfirm that the claimed invention of claim 86 is that of the above-stated predominant configuration where a controller 14 (e.g., a PLC or a computer) is connected to (and thus, services) multiple interface cards (e.g., two physical circuit packages 15), where each physical circuit package 15 is individually connected (via individual terminals 101-T_1 and 102-T_2) to a separate sensor or a separate actuator.

For all of these reasons, applicants respectfully submit that claims 86-90, do comply with the written description requirement and do contain subject matter which is described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventors, at the time the application was filed, had possession of the claimed invention, and meet all of the requirements of 35 USC 112, first paragraph.

d) In regard to the "Grounds of Rejection" section 6d, which are the rejections of claims 86-90 under 35 USC 112, second paragraph, the Examiner asserts that claim 86 recites that each controller is capable of "simultaneously" receiving a condition from a sensor and sending commands to an actuator. The Examiner asserts that the term "simultaneously" is a relative term which renders the claim indefinite.

The Examiner asserts that the term "simultaneously" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The Examiner asserts that in Remarks filed 5/9/05, applicants attempt to make a distinction between the sequential processing of the prior art (applicants note that it appears that the Examiner concedes that the prior art, i.e. McLeish and Sitte, utilize sequential processing and not simultaneous processing) and the claimed simultaneous processing. However, it is not clear to the Examiner that such a distinction is in fact proper, and the distinction does not appear to be supported by the original disclosure. Specifically, the Examiner asserts that at pg. 14, lines 25-27 it is recited:

"For each of the output modes corresponding input modes can be used simultaneously, specifically Mode I with Mode 2, Mode 4

with Mode 5 and Mode 6 with Mode 7. Within appropriate signal ranges different modes can be dynamically invoked ***sequentially*** (emphasis added)."

The Examiner asserts that this passage clearly suggests that the term "simultaneously" actually includes sequential operation of the modes. The Examiner notes that, as understood by one of ordinary skill in the art, sequential processing refers to the ability of a single processor to handle more than one task "simultaneously" by stepping through the different tasks in sequence. The Examiner asserts that parallel processing is another manner for handling multiple tasks simultaneously by handling each task on a separate processor. However, the Examiner asserts that the disclosure makes no mention of parallel processing and, indeed, discloses only a single processor in the controller. Therefore, the Examiner interprets that the term "simultaneously" includes sequential processing.

Applicants, however, traverse these rejections by asserting that claims 86-90 are definite and do particularly point out and distinctly claim the subject matter which applicants regard as the invention.

Specifically, applicants assert that the claimed invention of claims 86-90 distinctly claims subject matter found in the disclosure (see, for example, page 2, lines 4-6), which

defines a comprehensive interface circuit for automatic control of machines and processes to require an external controller in electrical communication with individual electronic interfaces for each sensor and for each actuator. With this configuration, the controller simultaneously senses inputs and actuates outputs (see, for example, page 3, lines 14-15 and Fig. 1). As Fig. 1 illustrates, and as one skilled in the art of using such PLC configurations of this type knows, the communication between the controller and each sensor and each actuator is direct, exclusive, and physical.

Applicants find that the above Examiner citation of the disclosure at page 14, lines 25-27 describes different internal (with respect to the physical circuit packages 15) control of the mode circuit 16! Thus, it appears to applicants that the Examiner is incorrectly applying the internal use of the words simultaneously and sequentially of the mode circuits 16 to the external (with respect to the physical circuit packages 15) control of claim 86. Applicants, however, traverse these assumptions by confirming that the word simultaneously of claim 86 is to be applied to the external control by the physical circuit package 15, as described at length in the previous paragraph.

Applicants find that the Examiner is correct in stating that applicants' Remarks of the 5/9/05 Amendment assert that the claimed invention claims simultaneous processing. Applicants also agree with the Examiner's concession that the prior art (i.e., McLeish and Sitte) disclose sequential processing. By virtue of at least these reasons, the claimed invention is distinguished from McLeish and Sitte.

By further concentrating on an incorrect embodiment that is not the claimed invention of claims 86-90, the Examiner next diverges to a discussion on parallel processing as a way of simultaneous processing. Applicants assert that claims 86-90 are not claiming parallel processing, as it applies to the external control of the two physical circuit packages 15, by the controller 14.

For all of these reasons, applicants respectfully submit that claims 86-90, are definite under 35 USC 112, second paragraph, and that the controller 14 is capable of simultaneously receiving a condition from each sensor and sending commands to each actuator of each of the physical packages that are connected to the controller.

e) In regard to the "Grounds of Rejection" section 6e, which are the rejections of claims 86-90 under 35 USC 103(a) as being unpatentable over McLeish in view of Sitte, the Examiner asserts that McLeish discloses a new comprehensive interface circuit for "simultaneously" sensing input and output devices, comprising:

a first physical circuit package (input-output device 2, Fig. 2) having a first electrical terminal, a second electrical terminal and a plurality of mode circuits disposed thereon, wherein said plurality of mode circuits can accomplish digital input, digital output, analog input, and analog output, and said first electrical terminal and said second electrical terminal being capable of electronic communication with each of said plurality of mode circuits (col. 4, lines 30-58; col. 5, lines 25-28);

a second physical circuit package (input-output device 2, Fig. 2) having a first electrical terminal, a second electrical terminal and a plurality of mode circuits disposed thereon, wherein said plurality of mode circuits can accomplish digital input, digital output, analog input, and analog output, and said first electrical terminal and said second electrical terminal being capable of electronic communication with each of said plurality of mode circuits (col. 4, lines 30-58; col. 5, lines 25-28); and

a controller (MP 3, Fig. 2) that is external to said first physical circuit package and said second physical circuit package, said controller capable of "simultaneously" receiving a condition from each sensor and being capable of "simultaneously" sending commands to each actuator (col. 3, line 52 - col. 4, line 3).

The Examiner then asserts that McLeish discloses "four terminals" for each "channel" (col. 4, lines 30-34). The Examiner asserts that nothing in McLeish requires that all four terminals be used for each connected device. Then the Examiner concedes that, nonetheless, McLeish does not specifically disclose that the physical circuit packages are electrically connected directly, exclusively, and physically to a single sensor or a single actuator, but not both simultaneously, via only first and second terminals. However, the Examiner asserts that Sitte teaches a sensor having two terminals (col. 1, lines 39-54, "U.S. Pat. No. ... over a wide range.").

The Examiner further asserts that such a "sensor" would inherently be coupled to a control circuit through only two terminals (e.g. first and second terminals). The Examiner concludes, therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify McLeish by electrically connecting the physical circuit packages directly, exclusively, and physically to single sensor or single actuator, but not both simultaneously, via only first and second terminals, because this would allow for coupling with a two-terminal sensor such as that disclosed by Sitte.

Applicants, however, traverse these rejections and assert that after studying the McLeish and Sitte references, applicants can find nowhere in the McLeish and/or Sitte references where the limitations of the claimed inventions of independent claim 86 are taught or suggested.

The Examiner concedes that McLeish discloses four terminals (see, Fig. 3, Term 1-3 and ground) for each field device 4. Applicants agree with this concession and assert that the claimed invention requires that there be no more than two terminals. Then the Examiner retracts this concession and asserts that nothing requires McLeish to use all four of these terminals for each field device.

Applicants disagree with this retraction and assert that various combinations of the four terminals are required by McLeish, depending on the exact type (e.g., output, input, analog, digital, current, voltage, etc.) of the field device being connected (see, for

example, the table at column 4, lines 36-48). This is contrary to the claimed invention, where only two terminals (101-T_1 and 102-T_2) are utilized.

Next, the Examiner concedes that, nonetheless, McLeish does not disclose that McLeish's field devices 4 are electrically connected directly, exclusively, and physically to single sensor or single actuator, but not both simultaneously, via only first and second terminals. Applicants also agree with these concessions and again find McLeish to be contrary to the claimed invention.

Then, the Examiner asserts that Sitte teaches a "sensor" having two terminals. Applicants find in this quote of Sitte (col. 1, lines 39-54), by the Examiner, that the sensor is a two terminal Hall sensor that is embedded in an integrated circuit. Applicants agree that there are many two terminal sensors, which would be equivalent to the sensors 70 of the claimed invention. However, a part of the discovery of the claimed invention is that the physical circuit package 15 has only two terminals, and that the physical circuit package 15 can interface these devices 70,72 (which could be a Hall sensor) to the controller 14.

Applicants assert that in the May 5, 2005 telephone interview between the Examiner and applicants counsel, it was applicants counsel's understanding that it was agreed that McLeish clearly requires "four" terminals to connect a field device 4 to a "channel" (see, for example, column 4, lines 30-34), but the claimed invention claims to interface sensors 70 and actuators 72 by way of only two terminals 101-T_1 and 102-T_2.

Applicants find McLeish and Sitte (see, for example, Fig. 1 in both references) having "bus topologies" that are clearly illustrated as such in both references' Fig. 1. These bus topologies are not the direct connections (see, for example, Fig. 1 of the present application) between each sensor 70 or each actuator 72, via the physical circuit packages 15, and the controller 14 of the claimed invention.

In addition, applicants draw attention to McLeish's Fig. 1 that represents the input-output device 2 (see, for example, column 3, lines 46-48) (which the Examiner asserts is analogous to the physical circuit package 15 of the claimed invention), where it is shown that up to 32 field devices 4 may be "multiplexed" (see MUX 16 in Fig. 1, i.e., input-output device 2). Clearly, the 32 field devices 4 shown in McLeish's Fig. 1 are not a single sensor or a single actuator that is electrically connected directly, exclusively, and physically to a physical circuit package of the claimed invention.

Thus, neither McLeish nor Sitte provide a controller which is capable of simultaneously receiving a condition from each sensor and capable of simultaneously sending commands to each actuator, as required by the claimed invention.

Further support for these assertions can be found in McLeish where McLeish teaches "sequentially sensing any input signals and providing any output signals" (see, for example, the Abstract) and the Sitte reference clearly utilizes "a digital bit stream" (see, for example, the Abstract and Fig. 1), where individual sensors and actuators are communicated in a "sequential" manner.

In contrast, the present application has a structure of a comprehensive interface circuit (see, for example, the Abstract) that comprises sensors 70 or actuators 72 that are in simultaneous communication (see, for example, page 3, lines 14-15 and Fig. 1), as in the above-discussed predominant PLC/computer configuration, with an external controller 14, via two physical circuit packages 15. The two terminals 101-T_1, 102-T_2 and the plurality of mode circuits 16 are disposed on each physical circuit package 15, where each set of terminals 101-T_1 and 102-T_2 are capable of being in electrical communication with their respective set of mode circuits 16, which can accomplish digital input, digital output, analog input, and analog output (see, for example, page 4, lines 17-19).

Each physical circuit package 15 is electrically connected directly (i.e., by way of individual connections 74-77), exclusively (i.e., there are no other connections attached to terminals 101-T_1 and 102-T_2, see, for example, Fig. 1), and physically (i.e., there is no electrical/electronic bus nor a wireless means illustrated in Fig. 1 that connects to terminals 101-T_1 and 102-T_2).

The controller 14, which is external to the physical packages 15, is capable of simultaneously receiving a condition from each sensor and is capable of sending commands to each actuator (see, for example, page 3, lines 14-15 and page **4**, lines 4-12) as in the above-discussed PLC/computer configuration.

Applicants assert that since Sitte is clearly directed to a bus topology, and the claimed invention claims the predominant PLC topology, clearly Sitte does nothing to overcome that shortcoming of McLeish.

For all of these reasons, the applicants respectfully submit that independent claim 86 is patentable over McLeish in view of Sitte, as the inventions defined thereby are not suggested within either McLeish in view of Sitte, nor is there any suggestion or motivation to modify or combine these references' teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claim 86 should be allowed over McLeish in view of Sitte.

e1) As for claim 87, the Examiner asserts that McLeish discloses the comprehensive interface circuit of claim 86, wherein each physical circuit package further has a point controller disposed thereon (central processing unit 6, Fig. 1).

Applicant, however, asserts that since claim 86 is patentable over McLeish in view of Sitte, then claim 87, which depends directly from claim 86, is also patentable, at least on this basis. Consequently, claim 87 should be allowed over McLeish in view of Sitte.

e2) As for claim 88, the Examiner asserts that McLeish discloses the comprehensive interface circuit of claim 86, further comprising an electrical bridge (the

Examiner concedes to the fact that McLeish is directed to a bus topology by referring to "address bus 7," Fig. 1).

Applicant, however, asserts that since claim 86 is patentable over McLeish in view of Sitte, then claim 88, which depends directly from claim 86, is also patentable, at least on this basis.

In addition, after studying McLeish and specifically McLeish's address bus 7, applicants do not find the address bus 7 to be analogous to the claimed invention's electrical bridge 10, which provides a single electrical unidirectional circuit path to monitor sensors or to control actuators (see, for example, page 8, lines 5-10). On the other hand, applicants find that McLeish's address bus 7 functions to "select" the appropriate message in VRAM or shift registers 20 that corresponds to the field device 4 (see, for example, column 6, line 65 to column 7, line 2).

For all of these reasons, the applicants respectfully submit that claim 88 is patentable over McLeish in view of Sitte, as the inventions defined thereby are not suggested within either McLeish or Sitte, nor is there any suggestion or motivation to modify or combine these references' teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claim 88 should be allowed over McLeish in view of Sitte.

e3) As for claim 89, the Examiner asserts that McLeish discloses the comprehensive interface circuit of claim 86, further comprising a monoline serial interface

(the Examiner concedes to the fact that McLeish is directed to a bus topology by referring to "data bus 11," Fig. 1).

Applicant, however, asserts that since claim 86 is patentable over McLeish in view of Sitte, then claim 89, which depends directly from claim 86, is also patentable, at least on this basis.

In addition, after studying McLeish and specifically McLeish's data bus 11, applicants do not find the data bus 11 to be analogous to the claimed invention's monoline serial interface 1200 (see, for example, Fig. 16), which sequences a single I/O line port 1110 through the following states: (i) a low impedance output high, an active state, for transmitting data; (ii) a low impedance output low, an active state, for transmitting data, where the output low state can be held for a variable length of time dependent upon the output data a "1" or "0" for digital data or a plurality of values for analog data; (iii) return to output high to generate an edge which may be used as a SPI clock by the I/O Engine 15; (iv) high impedance input, a passive state for receiving data, which state will be maintained until the transmission of the next bit of output data (see, for example, page 23 lines 9-19).

Furthermore, since the monoline serial interface 1200 of the present application is the monoline serial interface of the Related Application (U.S. Patent Application 09/916,215 that is disclosed on page 1, lines 21-24), which recently was allowed by the U.S. Patent and Trademark Office and soon will be issued as a U.S. Patent, applicants

further assert that the McLeish's data bus 11 is not the monoline serial interface 1200 of the claimed invention.

For all of these reasons, applicants respectfully submit that claim 89 is patentable over McLeish in view of Sitte, as the inventions defined thereby are not suggested within either McLeish or Sitte, nor is there any suggestion or motivation to modify or combine these references' teachings in order to teach or suggest the claimed limitations, as required by 35 U.S.C. § 103. Consequently, claim 89 should be allowed over McLeish in view of Sitte.

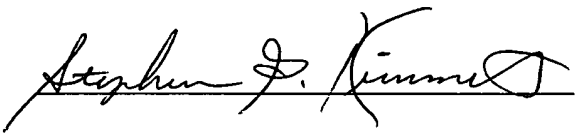
e4) As for claim 90, the Examiner asserts that McLeish discloses the comprehensive interface circuit of claim 86, wherein said first physical circuit package is electrically connected to a single sensor and said second physical circuit package is electrically connected to a single actuator (the Examiner further asserts that this embodiment clearly falls within the scope of McLeish's teachings, since McLeish teaches that any number of sensors or actuators may be attached to each input-output device. See col. 4, lines 23-29).

Applicant, however, asserts that since claim 86 is patentable over McLeish in view of Sitte, then claim 90, which depends directly from claim 86, is also patentable, at least on this basis. Consequently, claim 89 should be allowed over McLeish in view of Sitte.

CONCLUSION

For the foregoing reasons, it is submitted that the claims on appeal each define subject matter which is novel and would not have been obvious to one of ordinary skill in the art at the time the invention was made. Accordingly, all of the claims on appeal are believed to be entitled to allowance, and a favorable decision to that end is courteously solicited.

Respectfully submitted,



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CLAIMS APPENDIX

86. A comprehensive interface circuit for simultaneously sensing input devices and output devices, comprising:

a first physical circuit package having a first electrical terminal, a second electrical terminal and a plurality of mode circuits disposed thereon, wherein said plurality mode circuits can accomplish digital input, digital output, analog input, and analog output, said first physical circuit package being electrically connected directly, exclusively, and physically to a single sensor or a single actuator, but not both simultaneously, via only said first electrical terminal and said second electrical terminal of said first physical circuit package, and said first electrical terminal and said second electrical terminal being capable of electrical communication with each of said plurality of mode circuits;

a second physical circuit package having a first electrical terminal, a second electrical terminal and a plurality of mode circuits disposed thereon, wherein said plurality mode circuits can accomplish digital input, digital output, analog input, and analog output, said second physical circuit package being electrically connected directly, exclusively, and physically to another single sensor or another single actuator, but not both simultaneously, via only said first electrical terminal and said

second electrical terminal of said second physical circuit package, and said first electrical terminal and said second electrical terminal being capable of electrical communication with each of said plurality of mode circuits; and

a controller that is external to said first physical circuit package and said second physical circuit package, said controller being capable of simultaneously receiving a condition from each sensor and being capable of simultaneously sending commands to each actuator.

87. The comprehensive interface circuit of claim 86, wherein each physical circuit package further has a point controller disposed thereon.

88. The comprehensive interface circuit of claim 86, further comprising an electrical bridge.

89. The comprehensive interface circuit of claim 86, further comprising a monoline serial interface.

90. The comprehensive interface circuit of claim 86, wherein said first physical circuit package is electrically connected to a single sensor and said second physical circuit package is electrically connected to a single actuator.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None